METHOD AND APPARATUS FOR TIMING MANAGEMENT IN A CONVERTED DESIGN

ABSTRACT OF THE DISCLOSURE

Described is a method of converting one representation of a circuit into another. For example, a first network representation adapted for use with an FPGA can be converted into a second network representation adapted for use in a mask-programmable gate array. The method begins with accessing the first network representation, such as a netlist, and identifying signal paths that might be sensitive to race conditions. Representations of delay elements are then inserted into each sensitive signal path. The timing of the modified network representation is then modeled by calculating the delays associated with each signal path. Any differences in the modeled delay values are minimized by modifying one or more of the inserted delay-element representations. In one embodiment, the inserted delay-element representations include stopper cells that maintain the nets to and/or from the delay-element representations. Delay-element representations can therefore be modified without altering the circuit timing of related net segments.